ABSTRACT OF THE DISCLOSURE

The present invention discloses a ferroelectric random access memory having a multi-bit line structure. The ferroelectric random access memory includes a plurality of cell array blocks for storing cell data, a common data bus unit for transmitting read/write data, and a timing data register array unit for sensing the read data and outputting the write data to the common data bus unit. The timing data register array unit senses the read data by using timing of a sensing voltage of the common data bus unit to reach the sensing threshold voltage. As a result, the ferroelectric random access memory improves a sensing margin in a low voltage and increases a sensing speed.